UNIVERSITY DEPARTMENT OF PHYSICS

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M.SC. PHYSICS

SEMESTER - II

PAPER – 203: ELECTRONICS

MODEL QUESTIONS

Note: ***Students are advised to refer prescribed Text Books for Complete Answers.***

GROUP A

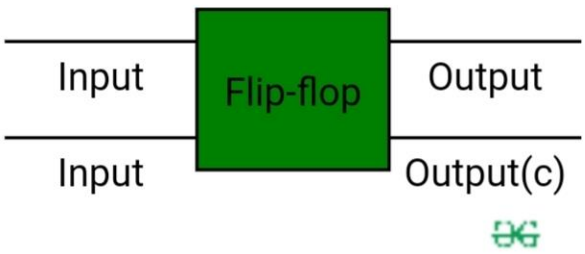
SHORT ANSWER TYPE QUESTIONS

1. **What is a flip-flop? What are the differences between a flip-flop and a latch?**

Flip-Flop :

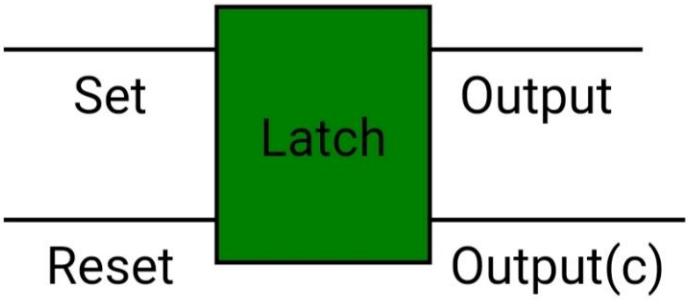
Flip-flop is a basic digital memory circuit, which stores one bit of information.Flip flops are the fundamental blocks of most sequential circuits. It is also known as a bistable multivibrator or a binary or one-bit memory. Flip-flops are used as memory elements in sequential circuit.

The output is obtained in a sequential circuit from combinational circuit or flip-flop or both. The state of flip-flop changes at active state of clock pulses and remains unaffected when the clock pulse is not active. In particular, clocked flip flops serve as memory elements in synchronous sequential Circuits and unclocked flip-flops (i.e., latches) serve as memory elements in asynchronous sequential circuits.



Latch :

Latch is an electronic device, which changes its output immediately based on the applied input. It is used to store either 1 or 0 at any specified time. It consists of two inputs namely "SET" and RESET and two outputs, which are complement to each other.



Difference between Flip-flop and Latch :

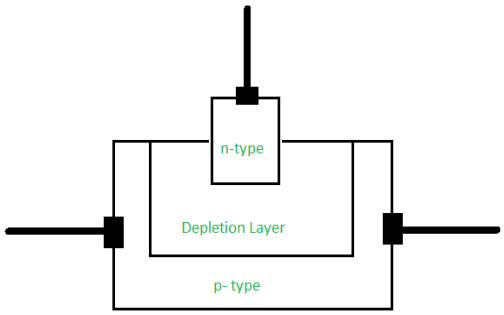
SNO	FLIP-FLOP	LATCH
1	Flip-flop is a bistable device i.e., it has two stable states that are represented as 0 and 1.	Latch is also a bistable device whose states are also represented as 0 and 1.
2	It checks the inputs but changes the output only at times defined by the clock signal or any other control signal.	It checks the inputs continuously and responds to the changes in inputs immediately.
3	It is a edge triggered device.	It is a level triggered device.
4	Gates like NOR, NOT, AND, NAND are building blocks of flip flops.	These are also made up of gates.
5	They are classified into asynchronous or synchronous flipflops.	There is no such classification in latches.
6	It forms the building blocks of many sequential circuits like counters.	These can be used for the designing of sequential circuits but are not generally preferred.
7	a Flip-flop always have a clock signal	latche doesn't have a clock signal
8	Flip-flop can be build from Latches	Latches can't build from gates
9	ex:D Flip-flop, JK Flip-flop	ex:SR Latch, D Latch

2. **What do you mean by poles and zeros?**

3. What is a MOSFET? How does it differ from a FET?

The **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass. **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

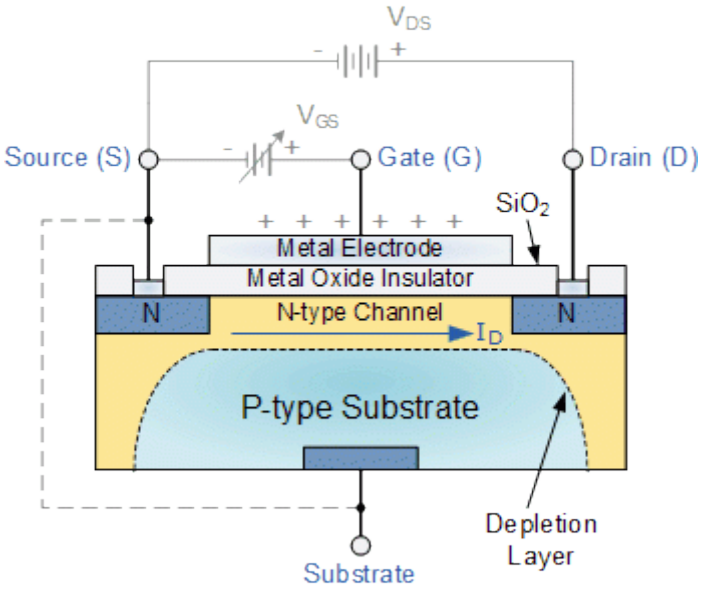
JFET (Junction Gate Field-Effect Transistor):
JFET is a field-effect transistor and it is the three terminal devices. There are number of application of that, it can be used as switch, amplifier, etc. It is classified into two categories: N-Channel JFET and P-Channel JFET.



JFET

MOSFET (Metal–Oxide–Semiconductor Field-Effect Transistor):

The MOSFET is a field-effect transistor and it is a four terminal device with source(S), gate (G), drain (D) and body (B) terminals. It's generally classified into two basic configurations: Depletion Mode MOSFET and Enhancement Mode MOSFET.



Difference between JFET and MOSFET

S.NO.	JFET	MOSFET
1	JFET(Junction Gate Field-Effect Transistor) is a three-terminal semiconductor device.	MOSFET(Metal–Oxide–Semiconductor Field-Effect Transistor) is a four-terminal semiconductor device.
2	It can only operates in the depletion mode.	It operates in both depletion mode and enhancement mode.
3	It has high input impedance on the order of 1010 ohms, therefore	It offers even higher input impedance than the JFETs,

S.NO.	JFET	MOSFET
	they are more sensitive towards input voltage signals.	therefore they are more resistive.
4	It allows the gate leakage current on the order of 10^{-9} A	While the gate leakage current for MOSFETs will be of the order of 10^{-12} A.
5	It is relatively cheaper than MOSFETs	It is expensive one.
6	These are ideal for low noise applications.	These are mainly used for high noise applications.
7	These are less susceptible to damage because of the high input capacitance.	These are more susceptible to damage because of the metal oxide insulator.
8	Manufacturing process of JFETs is simple.	Manufacturing process of MOSFETs is complex.

4. What is a current mirror? Explain the operation of a simple current mirror.

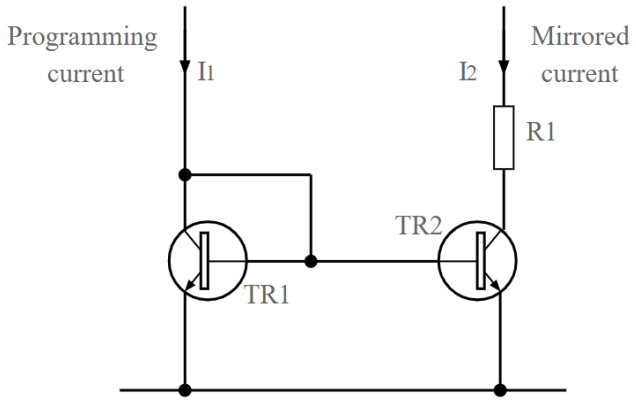
Current mirror circuits generally consist two main transistor, although other devices such as FETs can be used. Some current mirror circuits may use more than two transistors to enable the level of performance to be improved.

The current mirror circuit gains its name because it copies or mirrors the current flowing in one active device in another, keeping the output current constant regardless of loading. The current being mirrored can be a constant current, or it can be a varying signal dependent upon the requirement and hence the circuit.

Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits.

Current mirror circuit

The basic circuit of the transistor current mirror is shown in the diagram below. It comprises two transistors, one of which has the base and collector connected and the other does not. The base connections of both transistors are then linked, as are the emitters which are also taken to ground.



In terms of the operation of the circuit, the base emitter junction of TR1 acts like a diode because the collector and base are connected together.

The current into TRI is set externally by other components, and as a result there is a given voltage built up across the base emitter junction of TR1. As the base emitter voltage on both transistors is the same, the current in one transistor will exactly mirror that of the second, assuming that both transistors are accurately matched. Therefore the current flowing into TR1 will be mirrored into TR2 and hence into the load R1.

Circuit limitations

The two transistor current mirror circuit shown above is often quite adequate for most applications. However it has some noticeable limitations under many circumstances:

- ***Current varies with change in output voltage:*** This effect occurs because the output impedance is not infinite. This is because there is a slight variation of Vbe with the collector voltage at a given current in TR2. Often the current may vary by about 25% the output compliance range.
- ***Current matching dependent on transistor matching:*** The current mirroring is dependent upon the matching of the transistors. Often the transistors need to be on the same substrate if they are to accurately mirror the current.

6. What do you mean by a logic family? Describe the features of various logic families.

Different circuit configurations and production technologies are used during the production of digital integrated circuits. Each of these approaches is called a specific **Logic Families**. Now the idea of having different approaches or different logic families is that each ICs of same family when fabricated will have identical electrical characteristics. The characteristics which are bound to be identical are supply voltage range, speed of response, dissipation of power, input and output logic levels, current sinking capability, current sourcing capability, noise margin, fan-out etc.

Significance of Logic Families

When we talk about digital systems actually the digital ICs are the ones which make up the whole system. And if all the ICs are of same logic family then they are compatible to each other and the intended logic functions are performed and the goal is achieved.

But in case ICs belonging to **different logic families** are used in a digital system then to ensure compatibility interfacing techniques must be used. And that is the reason why we must understand different logic families and use the best combination

of ICs during the design of a digital system. Now the question arises what might be the consequence of choosing wrong combinations of ICs. The answer is that it may not match the necessary capability needed.

Types of Logic Family

The digital ICs are designed using any of either bipolar devices or MOS or a combination of both. The logic families which fall under the first kind are called bipolar families, this include diode logic (DL), emitted coupled logic (ECL), resistor transistor logic (RTL), diode transistor logic (DTL), transistor transistor logic (TTL). The members of other logic family i.e. MOS family are PMOS, NMOS family, CMOS family. Now the Bi-MOS logic family is the one that uses both bipolar and MOS devices. Of the above mentioned families DL, RTL and DTL are not used these days they have become obsolete. TTL, CMOS, ECL, NMOS and Bi-CMOS are the families which are still used.

Logic Families indicate the type of logic circuit used in the IC. The main types of logic families are:

- TTL(Transistor Transistor Logic)
- CMOS (Complementary MOS)
- ECL (Emitter Coupled Logic)

TTL subfamilies

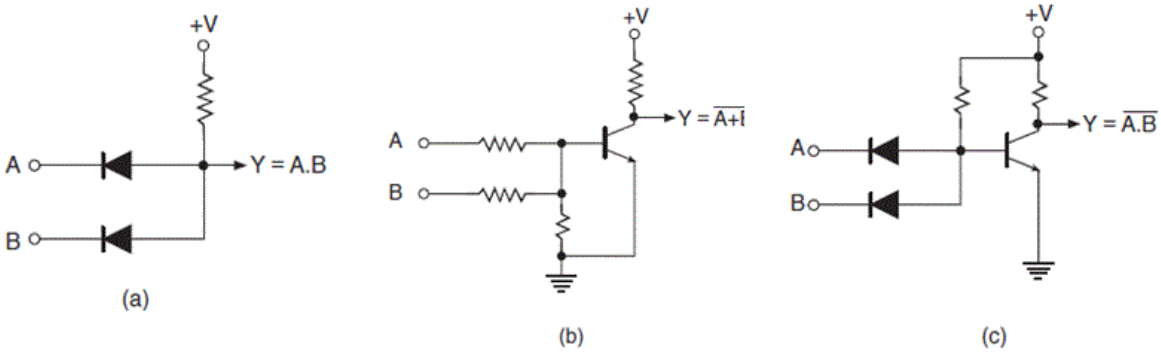
The TTL family consists of various subfamilies such as standard TTL, low-power TTL, high power TTL, low power Schottky TTL, Schottky TTL, advanced low-power Schottky TTL, advanced Schottky TTL and fast TTL. The ICs which belong to TTL family are designated as follows – 74 or 54 for standard TTL, 74L or 54L for low-power TTL, 74H or 54H for high power TTL, 74LS or 54LS for Low power schottky TTL and so on.

CMOS subfamilies

This is a popular logic family which includes 4000A, 4000B, 4000UB, 54/74C, 54/74HC, 54/74HCT, 54/74AC and 54/74ACT families. The subfamilies are divided on the basis of voltage difference and other parameters.

ECL Subfamilies

ECL stands for Emitter Coupled Logic family and it was introduced by ON semiconductor in 1962. The first product launched of this family was MECL-1 series. Later MECL-II, MECL-III, MECL-10K, MECL-10H series came into existence.



(a) Diode logic (b) resistor transistor logic and (c) diode transistor logic.

Characteristics of Logic Families

The main characteristics of Logic families include:

- Speed
- Fan-in
- Fan-out
- Noise Immunity
- Power Dissipation

Speed: Speed of a logic circuit is determined by the time between the application of input and change in the output of the circuit.

Fan-in: It determines the number of inputs the logic gate can handle.

Fan-out: Determines the number of circuits that a gate can drive.

Noise Immunity: Maximum noise that a circuit can withstand without affecting the output.

Power: When a circuit switches from one state to the other, power dissipates.

GROUP B

LONG ANSWER TYPE QUESTIONS

2. Explain the Routh-Hurwitz stability criterion.

3. Describe the construction and working of a UJT. Draw a neat circuit diagram of UJT as an oscillator and find an expression for its frequency of oscillation.

Unijunction Transistor (UJT)

A unijunction transistor (abbreviated as *UJT*) is a three-terminal semiconductor switching device. This device has a unique characteristic that when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply.Due to this characteristic, the unijunction transistor can be employed in a variety of applications *e.g.,* switching, pulse generator, saw-tooth generator etc.

The **Unijunction Transistor** or **UJT** for short, is another solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triac's for AC power control type applications.

Like diodes, unijunction transistors are constructed from separate P-type and N-type semiconductor materials forming a single (hence its name Uni-Junction) PN-junction within the main conducting N-type channel of the device.

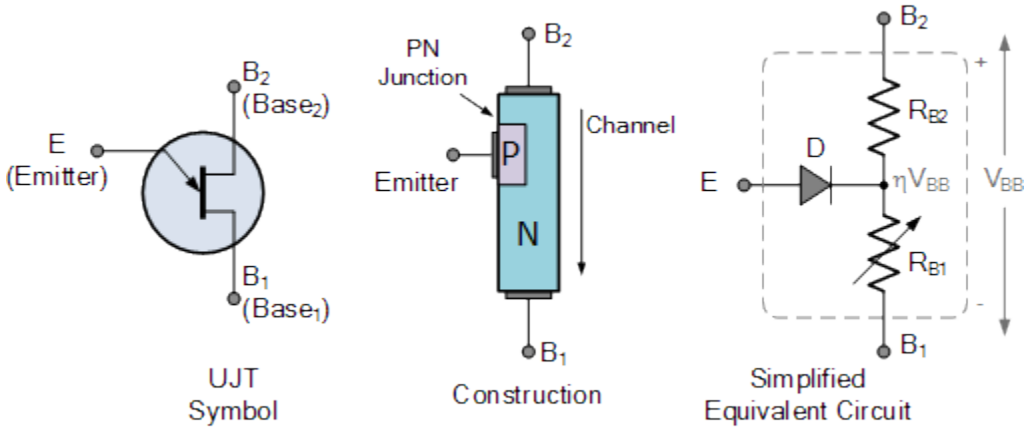
Although the *Unijunction Transistor* has the name of a transistor, its switching characteristics are very different from those of a conventional bipolar or field effect transistor as it can not be used to amplify a signal but instead is used as a ON-OFF switching transistor. UJT's have unidirectional conductivity and negative impedance characteristics acting more like a variable voltage divider during breakdown.

Like N-channel FET's, the UJT consists of a single solid piece of N-type semiconductor material forming the main current carrying channel with its two outer connections marked as *Base 2* (B_2) and *Base 1* (B_1). The third connection, confusingly marked as the *Emitter* (E) is located along the channel. The emitter terminal is represented by an arrow pointing from the P-type emitter to the N-type base.

The Emitter rectifying p-n junction of the unijunction transistor is formed by fusing the P-type material into the N-type silicon channel. However, P-channel UJT's with an N-type Emitter terminal are also available but these are little used.

The Emitter junction is positioned along the channel so that it is closer to terminal B_2 than B_1. An arrow is used in the UJT symbol which points towards the base indicating that the Emitter terminal is positive and the silicon bar is negative material. Below shows the symbol, construction, and equivalent circuit of the UJT.

Unijunction Transistor Symbol and Construction



#Note: Refer Text Book for complete Answer for this question

4. Explain the input and output characteristics of a BJT.

Input Characteristics :

It is the curve between input current I_Band input voltage〖 V〗_BEat constant collector-emitter voltage, V_BE. The base current is taken along Y-axis and V_BE is taken along X-axis. Fig shows the input characteristics of a typical transistor in common-emitter configuration.

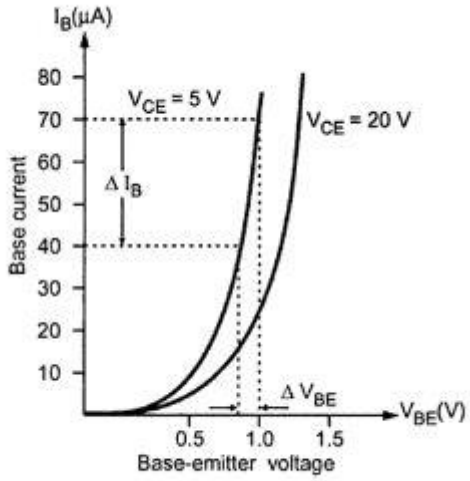


Fig 3.2: Input characteristics of the transistor in CE configuration

B) Output Characteristics:

This characteristic shows the relation between the collector current I_C and collector voltageV_CE, for various fixed values of〖 I 〗_B. This characteristic is often called collector characteristics.

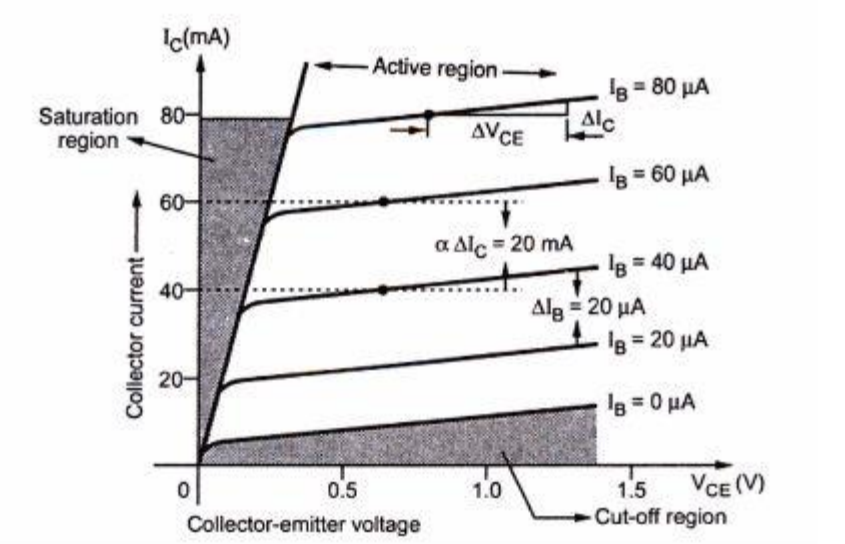


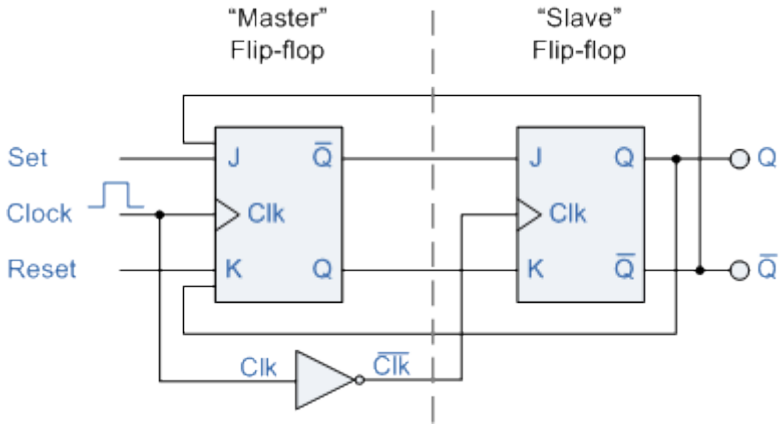
Fig 3.3: Output characteristics of the transistor in CE configuration

5. Design a difference amplifier using BJT and find an expression for its output.

6. Explain JK master-slave flip-flop.

Master-Slave Flip Flop Circuit

Master-slave flip flop is designed using two separate flip flops. Out of these, one acts as the master and the other as a slave. The figure of a master-slave J-K flip flop is shown below.

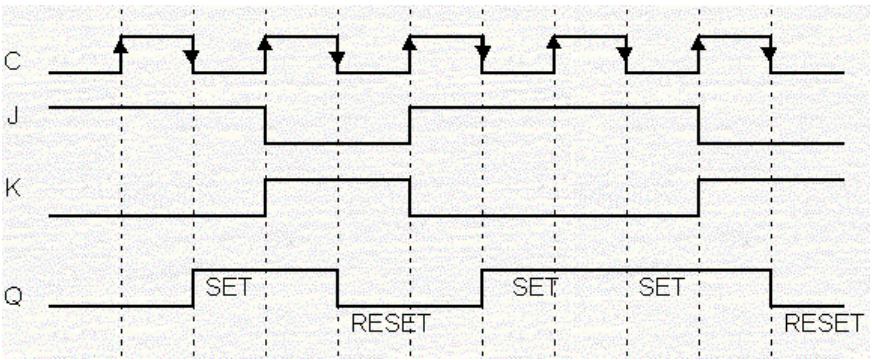


From the above figure it can be seen that both the J-K flip flops are presented in a series connection. The output of the master J-K flip flop is fed to the input of the slave J-K flip flop. The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop. The clock pulse [Clk] is given to the master J-K flip flop and it is sent through a NOT Gate and thus inverted before passing it to the slave J-K flip flop.

Thus, the circuit accepts the value in the input when the clock is HIGH, and passes the data to the output on the falling-edge of the clock signal. This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.

Working

When Clk=1, the master J-K flip flop gets disabled. The Clk input of the master input will be the opposite of the slave input. So the master flip flop output will be recognized by the slave flip flop only when the Clk value becomes 0. Thus, when the clock pulse males a transition from 1 to 0, the locked outputs of the master flip flop are fed through to the inputs of the slave flip-flop making this flip flop edge or pulse-triggered. To understand better take a look at the timing diagram illustrated below.



Thus, the circuit accepts the value in the input when the clock is HIGH, and passes the data to the output on the falling-edge of the clock signal. This makes

the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.

7. What is a counter? Explain the operation of a ripple counter with a neat diagram.

A **counter** is basically used to count the number of clock pulses applied to a flip-flop. It can also be used for Frequency divider, time measurement, frequency measurement, distance measurement and also for generating square waveforms. In this, the flip-flops are asynchronous counters and are supplied with different clock signals, there may be a delay in producing output.
Also, a few numbers of logic gates are needed to design asynchronous counters. So they are elementary in design and also are less expensive.

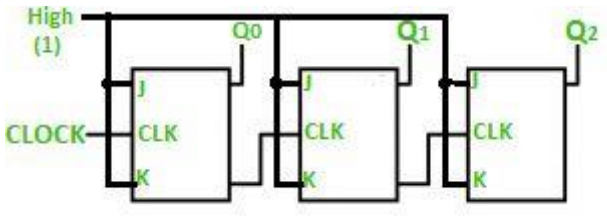
Ripple counter –

A n-bit ripple counter can count up to 2^n states. It is also known as MOD n counter. It is known as ripple counter because of the way the clock pulse ripples its way through the flip-flops. Some of the features of ripple counter are:

1. It is an asynchronous counter.
2. Different flip-flops are used with a different clock pulse.
3. All the flip-flops are used in toggle mode.
4. Only one flip-flop is applied with an external clock pulse and another flip-flop clock is obtained from the output of the previous flip-flop.
5. The flip-flop applied with external clock pulse act as LSB (Least Significant Bit) in the counting sequence.

A counter may be an up counter that counts upwards or can be a down counter that counts downwards or can do both i.e.count up as well as count downwards depending on the input control. The sequence of counting usually gets repeated after a limit. When counting up, for n-bit counter the count sequence goes from 000, 001, 010, … 110, 111, 000, 001, … etc. When counting down the count sequence goes in the opposite manner: 111, 110, … 010, 001, 000, 111, 110, … etc.

A 3-bit Ripple counter using JK flip-flop –



In the circuit shown in above figure, Q0(LSB) will toggle for every clock pulse because JK flip-flop works in toggle mode when both J and K are applied 1, 1 or high input. The following counter will toggle when the previous one changes from 1 to 0.

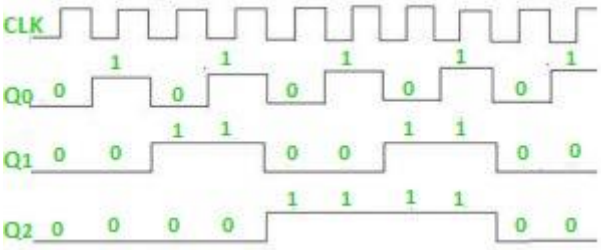
Truth Table –

Counter State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The 3-bit ripple counter used in the circuit above has eight different states, each one of which represents a count value. Similarly, a counter having n flip-flops can have a maximum of 2 to the power n states. The number of states that a counter owns is known as its mod (modulo) number. Hence a 3-bit counter is a mod-8 counter.

A mod-n counter may also be described as a divide-by-n counter. This is because the most significant flip-flop (the furthest flip-flop from the original clock pulse) produces one pulse for every n pulses at the clock input of the least significant flip-flop (the one triggers by the clock pulse). Thus, the above counter is an example of a divide-by-4 counter.

Timing diagram – Let us assume that the clock is negative edge triggered so above counter will act as an up counter because the clock is negative edge triggered and output is taken from Q.



Counters are used very frequently to divide clock frequencies and their uses mainly involve in digital clocks and in multiplexing. The widely known example of the counter is parallel to serial data conversion logic.

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